IN THE CLAIMS:

Please amend the claims as indicated below.

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1. (Currently Amended) A cache memory, comprising:

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a plurality of sets of cache frames for storing information from main memory; and

a cache allocation system for allocating one or more sets of said cache memory to one or more tasks, wherein one or more secondary tasks may use only said allocated sets of said cache memory.

2. (Currently Amended) The cache memory of claim 1, ~~wherein one or more secondary tasks may use only said allocated sets of said cache memory and~~ wherein one or more primary tasks may use unallocated sets of said cache memory.

3. (Original) The cache memory of claim 1, further comprising a mapper that transforms a set index, A, identifying a set in said cache memory to a mapped set index, a, identifying a set with said allocated portion of said cache memory.

4. (Original) The cache memory of claim 1, wherein said allocated sets of said cache memory can be varied by selecting an appropriate map function.

5. (Original) The cache memory of claim 4, wherein said map function is a logical and function and wherein a given set of said cache memory is allocated to a given task by assigning said set a predefined binary value.

6. (Original) The cache memory of claim 1, further comprising a map register for identifying said one or more sets of said cache memory allocated to each task.

7. (Original) The cache memory of claim 1, wherein a size of said allocated one or more sets of said cache memory may be specified using a size select value.

8. (Original) The cache memory of claim 1, wherein one of said allocated sections of sets of said cache memory may be specified using a section select value.

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9. (Original) The cache memory of claim 1, wherein a desired location and size of said allocated sections of sets of said cache memory may be specified.

10. (Currently Amended) A method for allocating space in a cache memory, said method comprising the steps of:

storing information from main memory in a plurality of sets of said cache memory; and

allocating one or more of said sets of said cache memory to one or more tasks, wherein one or more secondary tasks may use only said allocated sets of said cache memory.

11. (Currently Amended) The method of claim 10, ~~wherein one or more secondary tasks may use only said allocated sets of said cache memory and~~ wherein one or more primary tasks may use unallocated sets of said cache memory.

12. (Original) The method of claim 10, further comprising the step of transforming a set index, A, identifying a set in said cache memory to a mapped set index, a, identifying a set with said allocated portion of said cache memory.

13. (Original) The method of claim 10, further comprising the step of selecting an appropriate map function to vary said allocated sets of said cache memory.

14. (Original) The method of claim 13, wherein said map function is a logical and function and further comprising the step of allocating a given set of said cache memory to a given task by assigning said set a predefined binary value.

15. (Original) The method of claim 10, further comprising the step of identifying said one or more sets of said cache memory allocated to each task.

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16. (Original) The method of claim 10, further comprising the step of specifying a size of said allocated one or more sets of said cache memory.

17. (Original) The method of claim 10, further comprising the step of specifying one of said allocated sections of sets of said cache memory.

18. (Original) The method of claim 10, further comprising the step of specifying a desired location and size of said allocated section of sets of said cache memory.

19. (Currently Amended) A cache memory, comprising:

means for storing information from main memory in a plurality of sets of said cache memory; and

means for allocating one or more of said sets of said cache memory to one or more tasks, wherein one or more secondary tasks may use only said allocated sets of said cache memory.

20. (Original) The cache memory of claim 19, further comprising means for transforming a set index, A, identifying a set in said cache memory to a mapped set index, a, identifying a set with said allocated portion of said cache memory.

21. (Original) The cache memory of claim 19, wherein said allocated sets of said cache memory can be varied by selecting an appropriate map function.

22. (Original) The cache memory of claim 21, wherein said map function is a logical and function and wherein a given set of said cache memory is allocated to a given task by assigning said set a predefined binary value.

23. (Original) The cache memory of claim 19, further comprising means for identifying said one or more sets of said cache memory allocated to each task.

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24. (Original) The cache memory of claim 19, wherein a desired location and size of said allocated sections of sets of said cache memory may be specified.

25. (Currently Amended) An integrated circuit, comprising:

a cache memory having a plurality of sets of cache frames for storing information from main memory; and

a cache allocation system for allocating one or more sets of said cache memory to one or more tasks, wherein one or more secondary tasks may use only said allocated sets of said cache memory.

26. (Currently Amended) The integrated circuit of claim 25, ~~wherein one or more secondary tasks may use only said allocated sets of said cache memory and~~ wherein one or more primary tasks may use unallocated sets of said cache memory.

27. (Original) The integrated circuit of claim 25, further comprising a mapper that transforms a set index, A, identifying a set in said cache memory to a mapped set index, a, identifying a set with said allocated portion of said cache memory.

28. (Original) The integrated circuit of claim 25, wherein said allocated sets of said cache memory can be varied by selecting an appropriate map function.

29. (Original) The integrated circuit of claim 25, further comprising a map register for identifying said one or more sets of said cache memory allocated to each task.

30. (Original) The integrated circuit of claim 25, wherein a desired location and size of said allocated sections of sets of said cache memory may be specified.